# Introduction

This document lists the requirements for the GMII\_MAC\_Filter\_Sniffer FPGA core.

# GMII Interface

## MII

## GMII

# FPGA Bus Interface

## APB

# Internal Registers

# Clock Domains

MII and GMII interfaces operate on 25Mhz and 125Mhz clock frequencies. Most of my FPGA designs operate at 100Mhz. Therefore, a Clock Domain Crossing must occur between the data from the Ethernet busses and the internal logic.

# Internal Data Buffer

## FIFO